In the Abstract:

Amend the abstract as follows:

A method ~~for enabling~~ generates test vectors ~~to be generated~~ for a customer designed integrated circuit ~~(16)~~ having an embedded vendor circuit ~~(12) is disclosed~~. The embedded vendor circuit ~~(12)~~ has a proprietary circuit ~~(18)~~ and a nonproprietary circuit ~~(20)~~. At least one pseudo input is defined ~~(62)~~ to represent a portion of the nonproprietary circuit ~~(20)~~ to emulate the nonproprietary circuit output. An output node ~~(31)~~ of the embedded vendor circuit ~~(12)~~ to which an input of the customer designed circuit ~~(14)~~ is connectable is identified ~~(64)~~. A test netlist is created ~~(66)~~ which represents circuitry that produces output states at the output node ~~(31)~~ which would be generated by the embedded vendor circuit thereat ~~(12)~~. The test netlist includes at least one pseudo input and the output node, without including a full netlist of either the proprietary or nonproprietary circuits, and can be used to generate ~~(72)~~ scan test vectors for the customer designed integrated circuit ~~(14)~~ by the automatic test vector generating software program.